FIG. 1

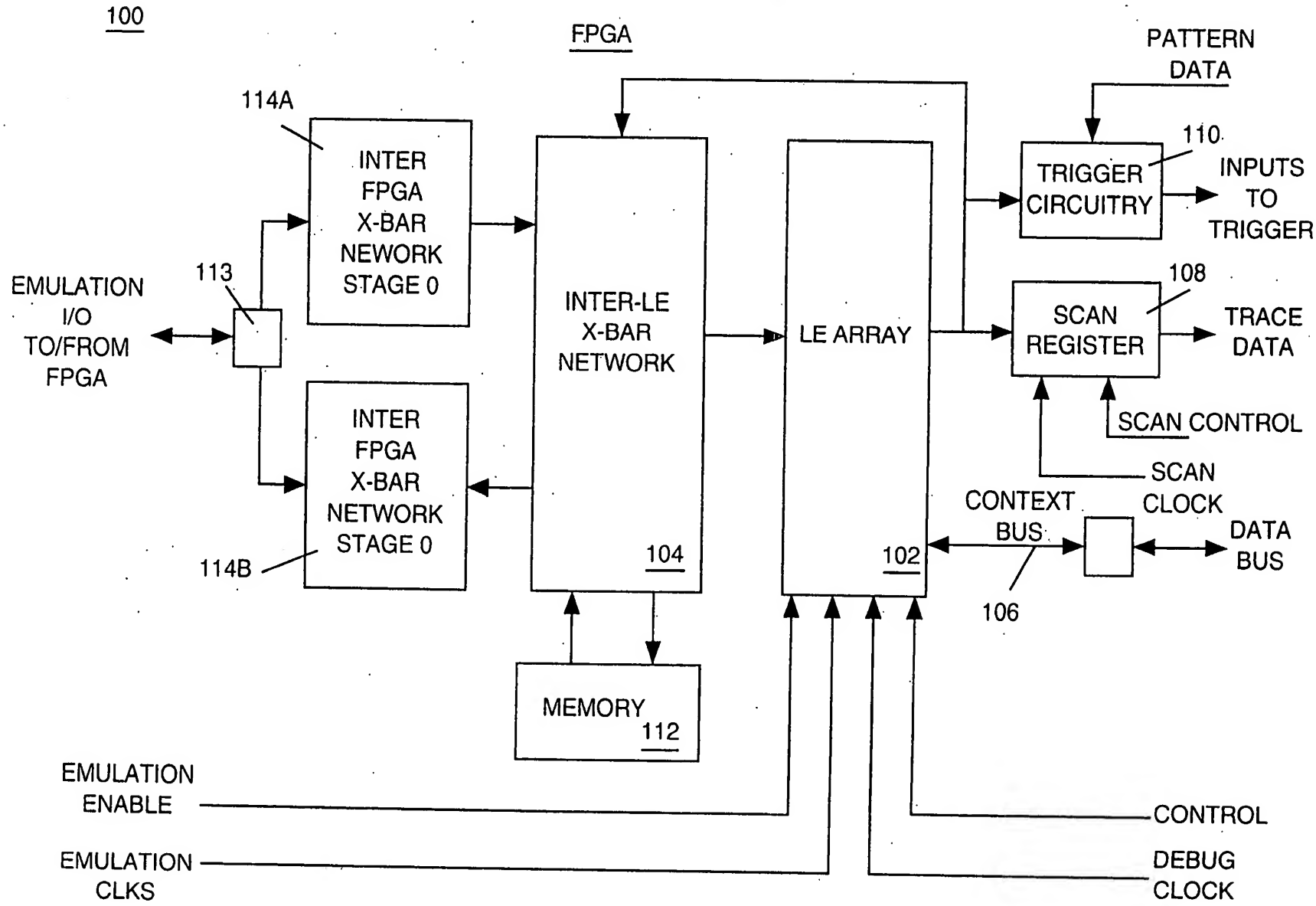


FIG. 2

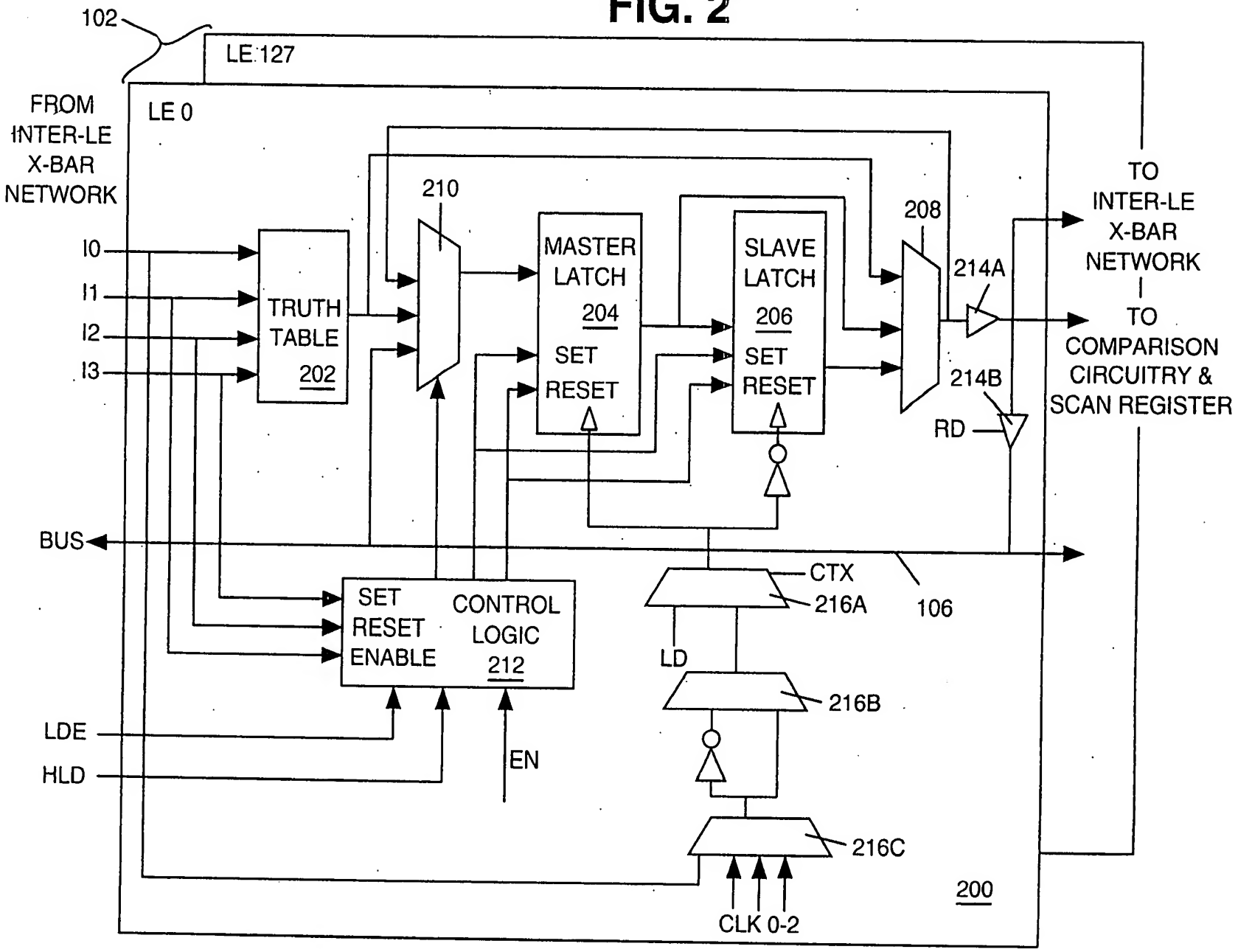

102
LE 127
LE 0
FROM INTER-LE X-BAR NETWORK
I0
I1
I2
I3
TRUTH TABLE 202
210
MASTER LATCH 204
SET
RESET
SLAVE LATCH 206
SET
RESET
208
214A
214B
RD
TO INTER-LE X-BAR NETWORK
TO COMPARISON CIRCUITRY & SCAN REGISTER
BUS
106
CTX
216A
LD
216B
216C
SET
RESET
ENABLE
CONTROL LOGIC 212
LDE
HLD
EN
CLK 0-2
200

FIG. 3

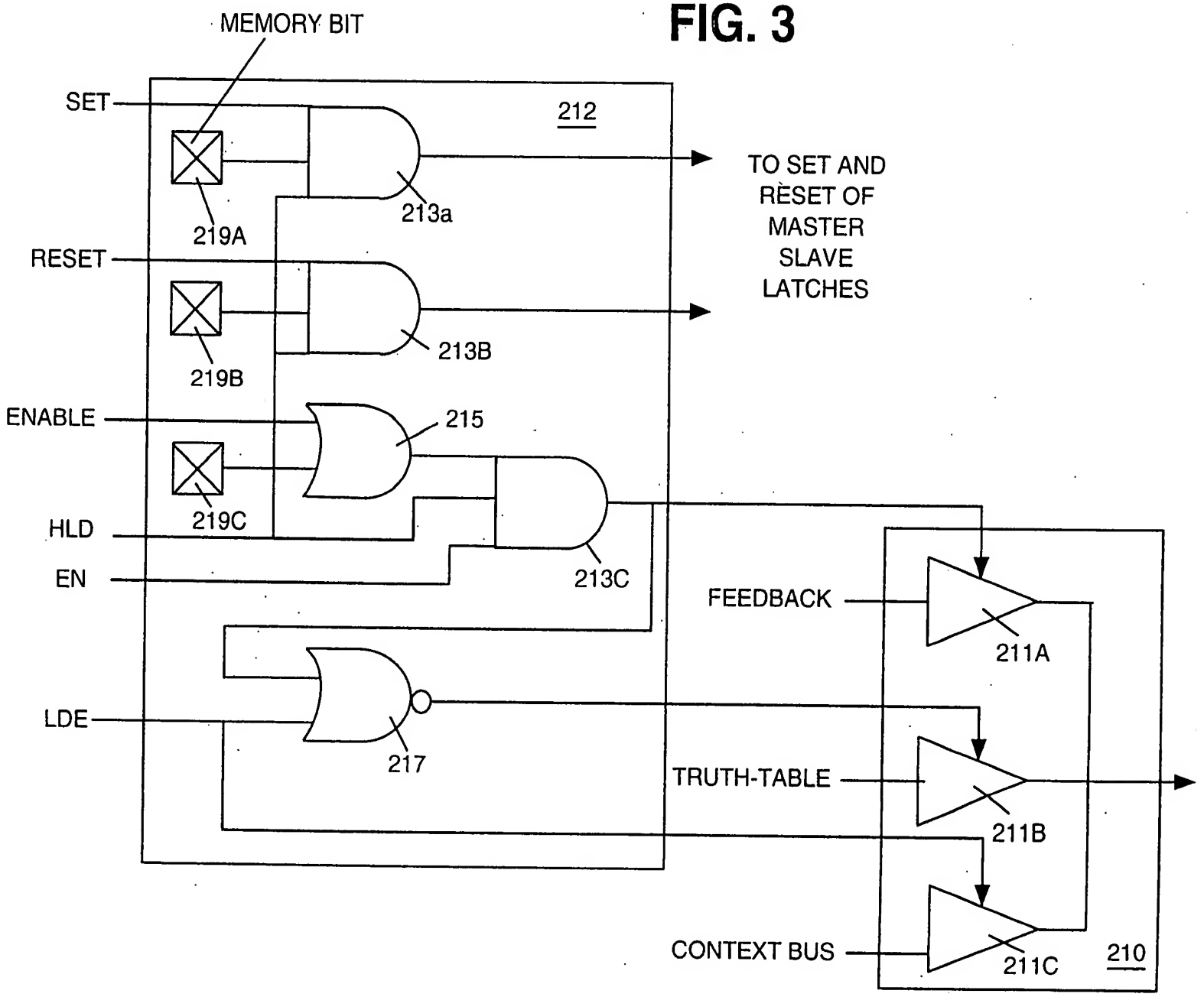

MEMORY BIT
SET
RESET
ENABLE
HLD
EN
LDE
219A
219B
219C
212
213a
213B
215
213C
217
TO SET AND RESET OF MASTER SLAVE LATCHES
FEEDBACK
TRUTH-TABLE
CONTEXT BUS
211A
211B
211C
210

FIG. 4A

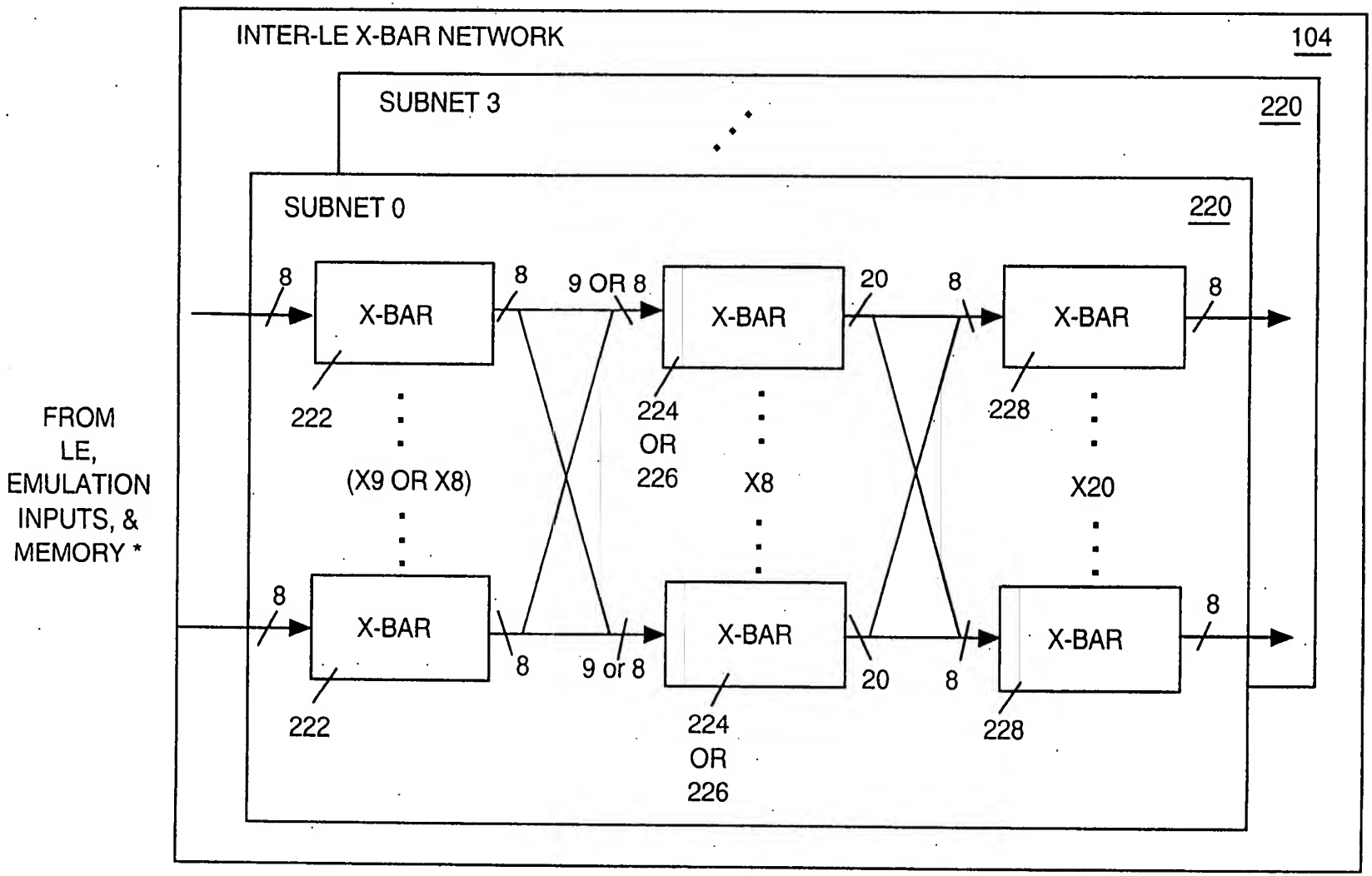

INTER-LE X-BAR NETWORK
104
SUBNET 3
220
SUBNET 0
220
FROM LE, EMULATION INPUTS, & MEMORY *
8
X-BAR
8
9 OR 8
X-BAR
20
8
X-BAR
8
222
(X9 OR X8)
224 OR 226
X8
228
X20
8
X-BAR
8
9 or 8
X-BAR
20
8
X-BAR
8
222
224 OR 226
228
* FOR 2 OR 4 OF THE SUBNETS

FIG. 4B

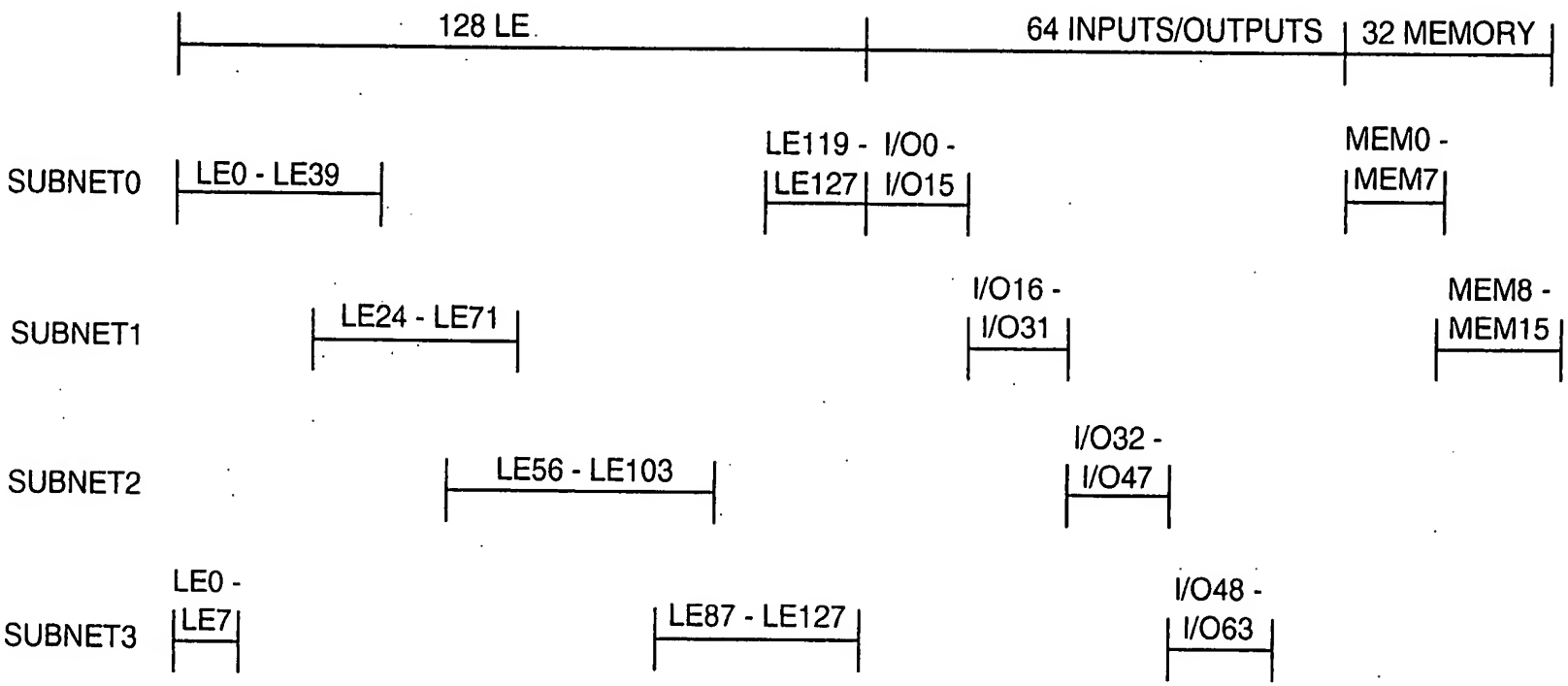

128 LE
64 INPUTS/OUTPUTS
32 MEMORY
SUBNET0
LE0 - LE39
LE119 - LE127
I/O0 - I/O15
MEM0 - MEM7
SUBNET1
LE24 - LE71
I/O16 - I/O31
MEM8 - MEM15
SUBNET2
LE56 - LE103
I/O32 - I/O47
SUBNET3
LE0 - LE7
LE87 - LE127
I/O48 - I/O63

FIG. 5

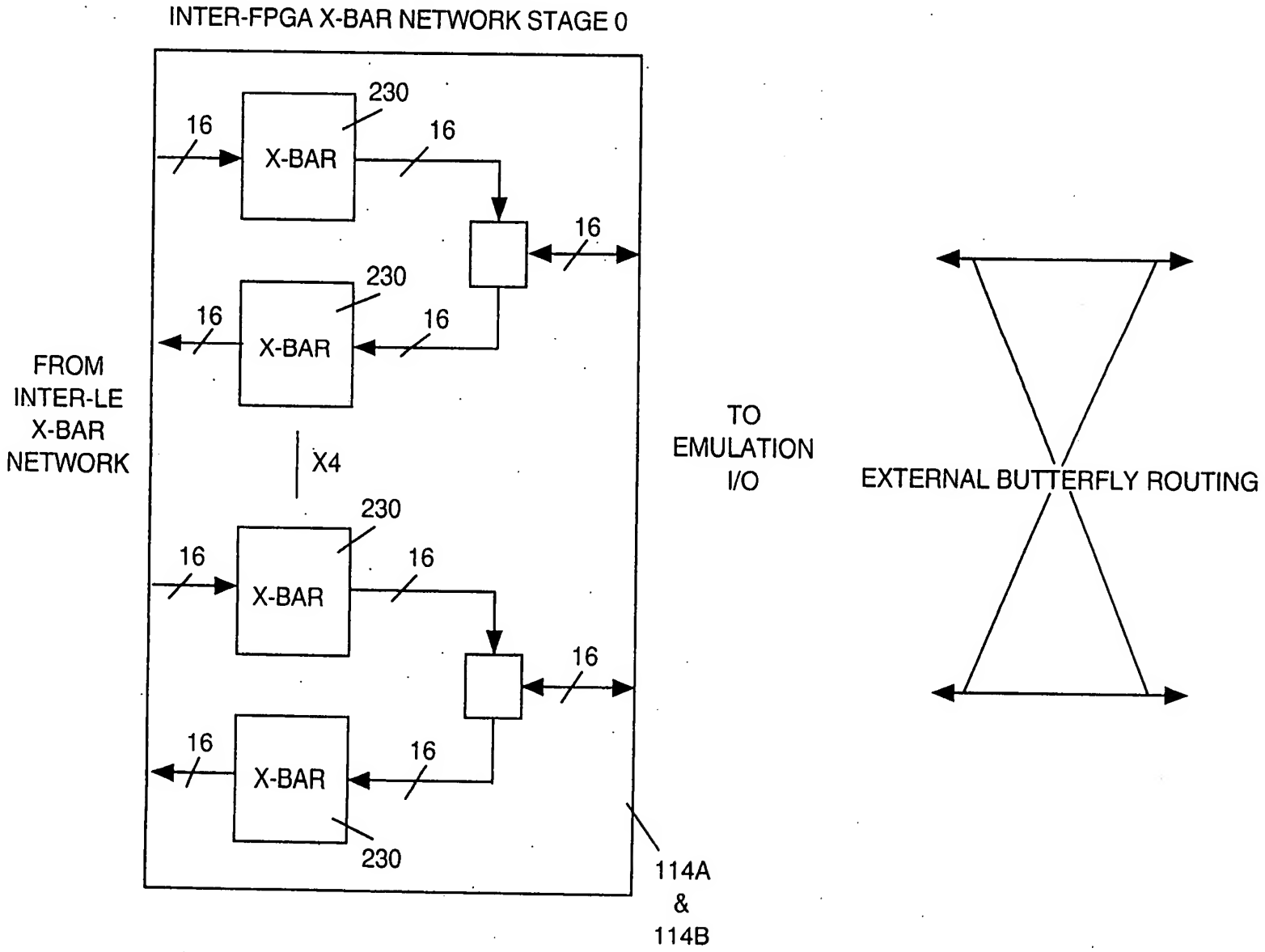

INTER-FPGA X-BAR NETWORK STAGE 0
230
16
X-BAR
16
16
230
16
X-BAR
16
FROM
INTER-LE
X-BAR
NETWORK
X4
TO
EMULATION
I/O
230
16
X-BAR
16
16
16
X-BAR
16
230
114A
&
114B
EXTERNAL BUTTERFLY ROUTING

FIG. 6

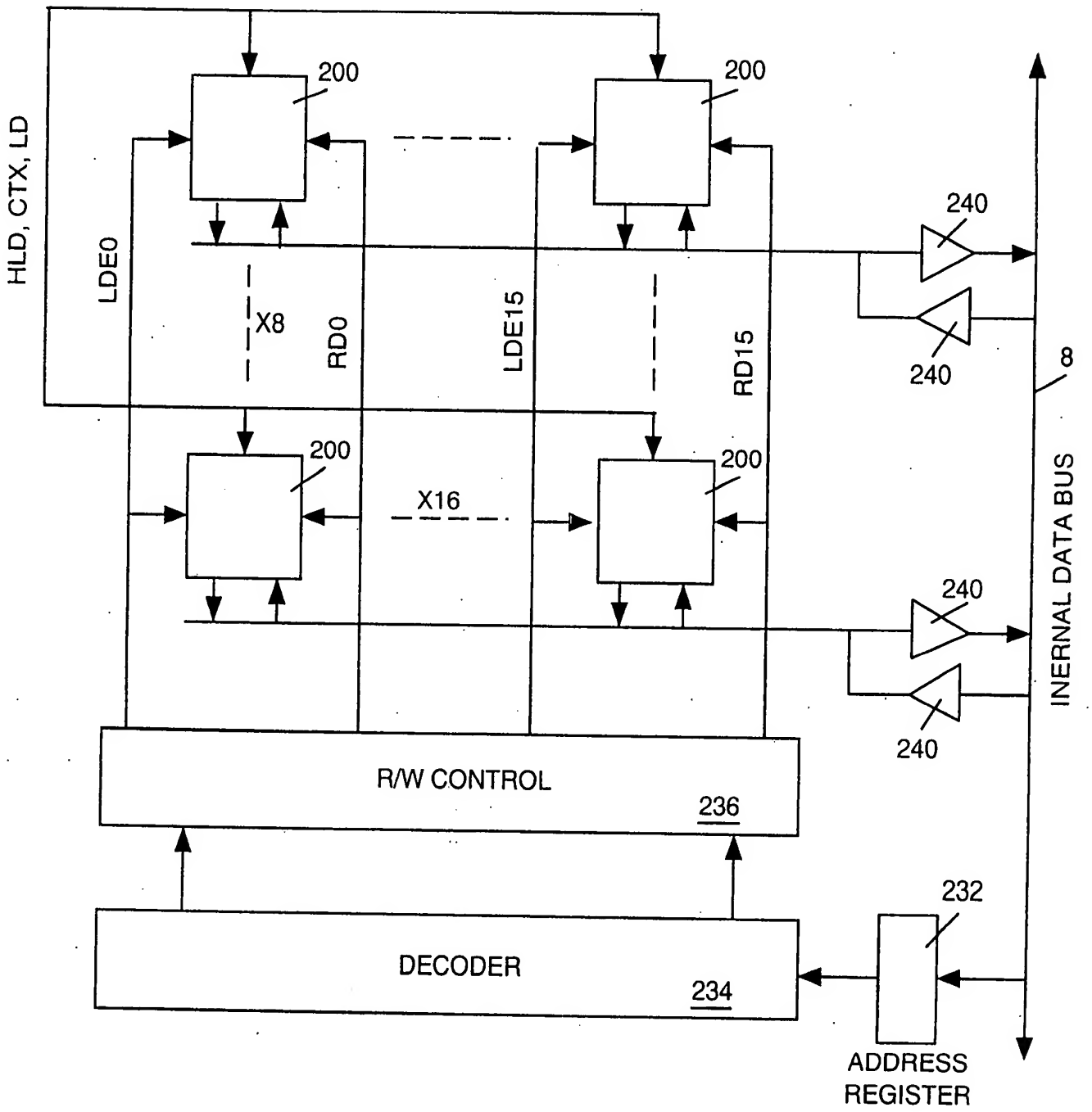

HLD, CTX, LD
LDE0
LDE15
RD0
RD15
X8
X16
200
200
200
200
240
240
240
240
8
INERNAL DATA BUS
R/W CONTROL
236
DECODER
234
232
ADDRESS
REGISTER

FIG. 7A

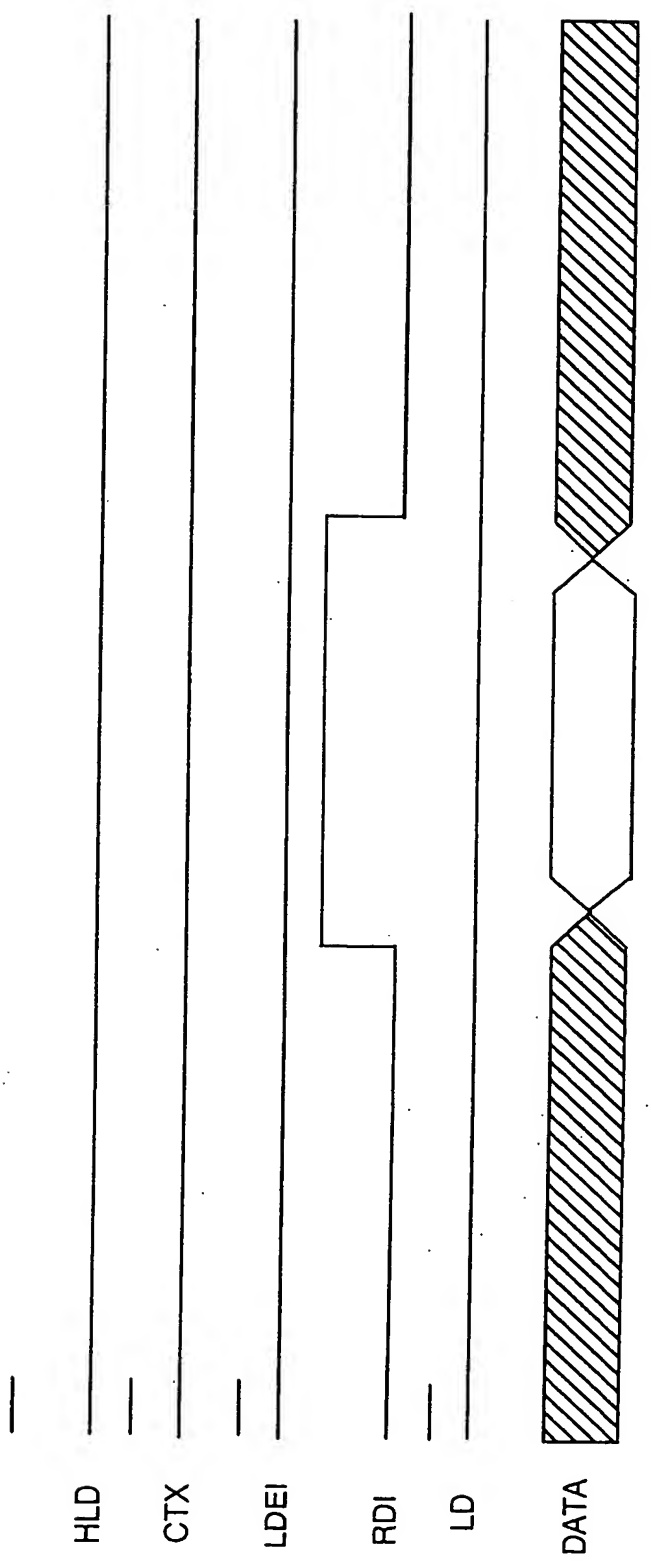


FIG. 7B

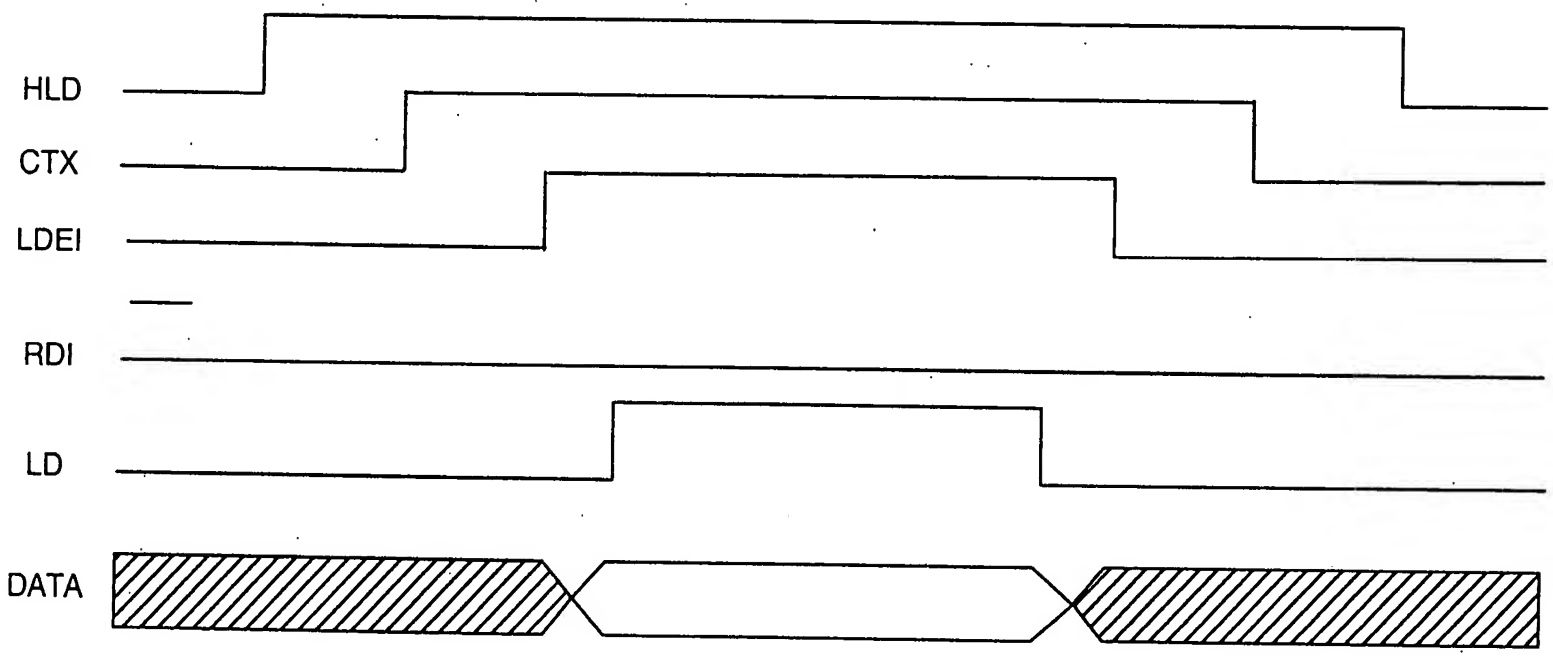


FIG. 8

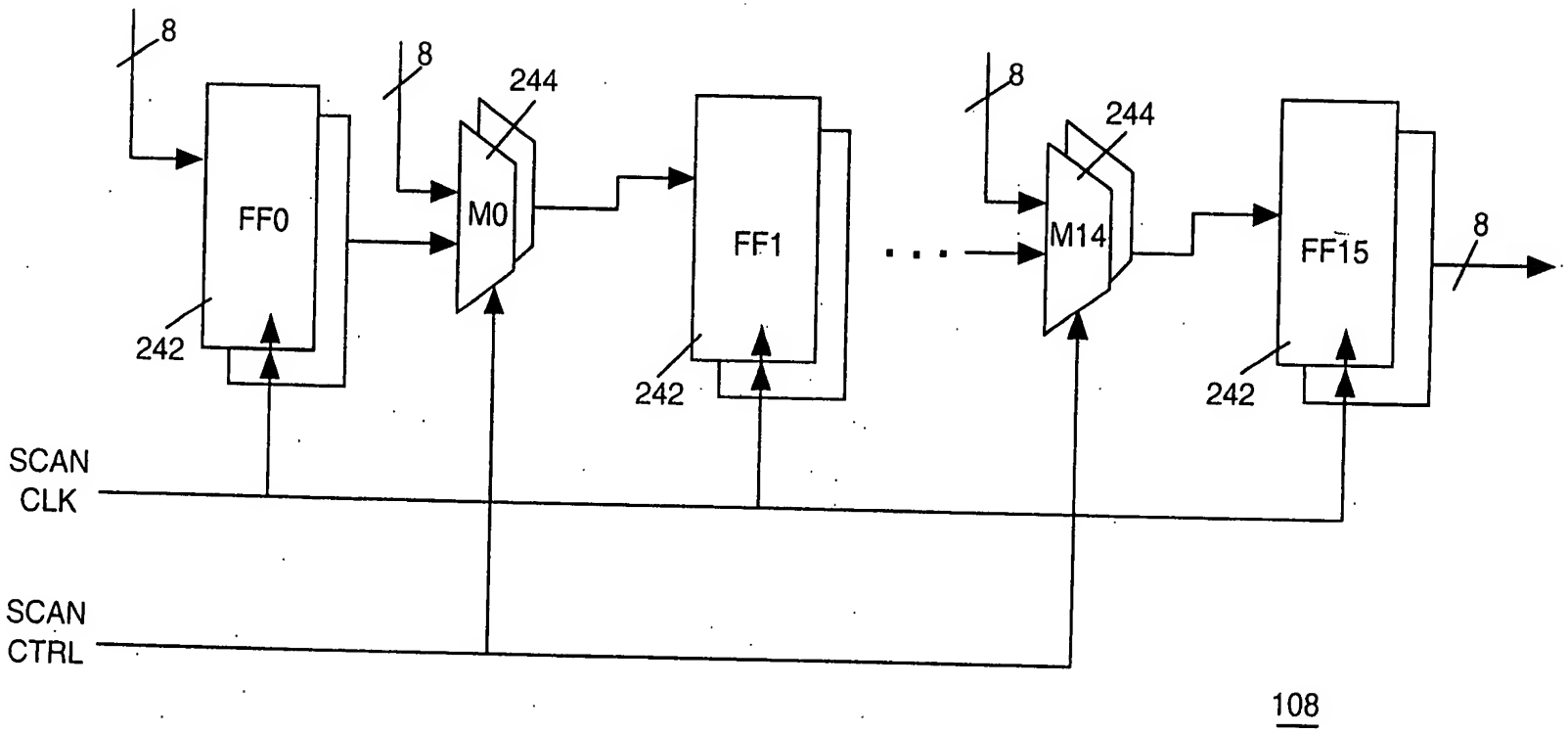
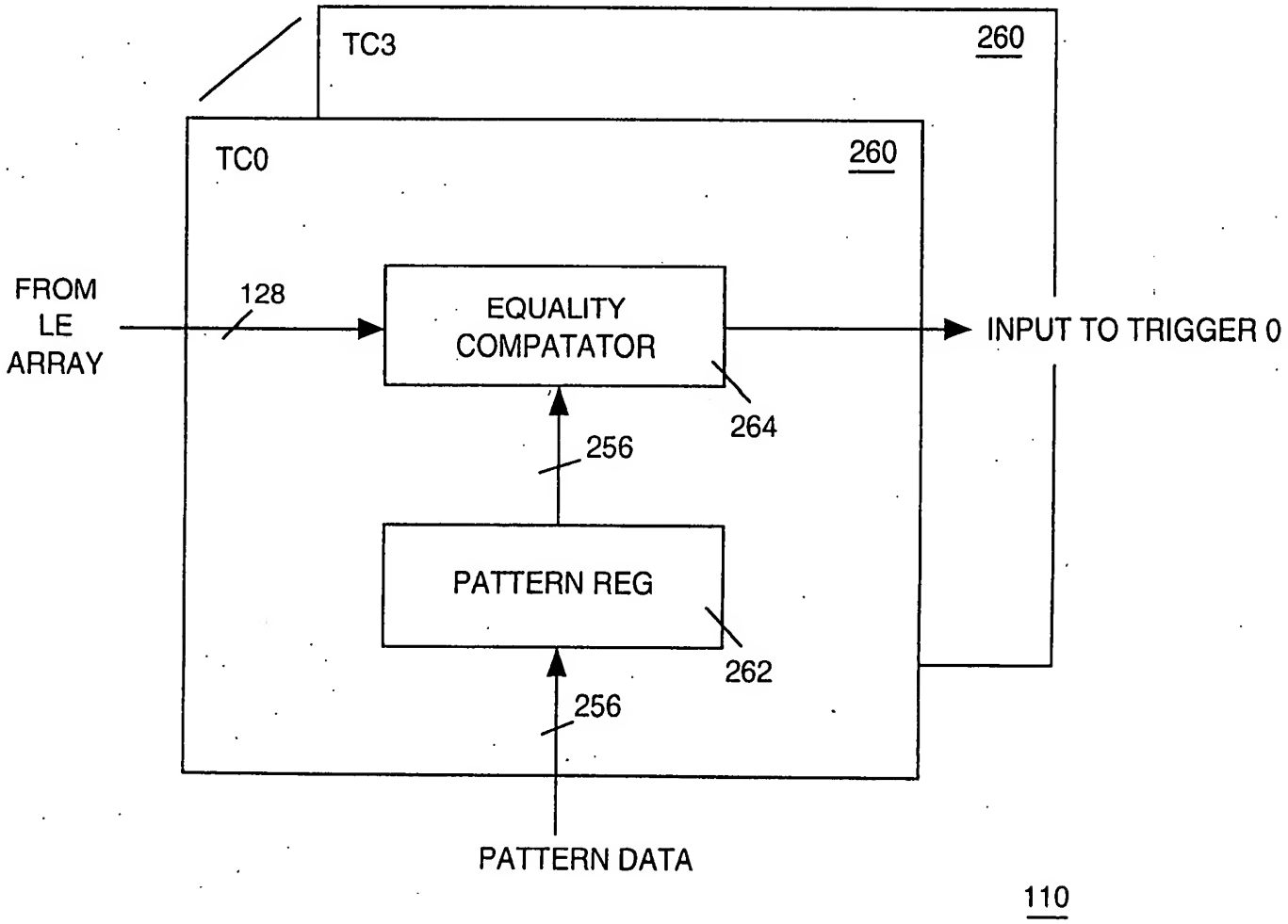

8
8
244
8
244
FF0
M0
FF1
M14
FF15
8
242
242
242
SCAN
CLK
SCAN
CTRL
108

FIG. 9


TC3
260
TC0
260
FROM
LE
ARRAY
128
EQUALITY
COMPATATOR
264
INPUT TO TRIGGER 0
256
PATTERN REG
262
256
PATTERN DATA
110